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Mira Albert, Maria del Carmen; Knott, Arnold; Andersen, Michael A. E.

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Analysis and Comparison of Magnetic Structures in a Tapped Boost Converter for LED Applications

Maria C. Mira, Arnold Knott, Michael A. E. Andersen
Dept. Electrical Engineering
Technical University of Denmark
Oersteds Plads, 349. Kongens Lyngby, Denmark
mmial@elektro.dtu.dk akn@elektro.dtu.dk ma@elektro.dtu.dk

***Abstract*— This paper presents an analysis and comparison of magnetics structures in a tapped boost converter for LED applications. The magnetic structure is a coupled inductor which is analyzed in a conventional wire-wound core as well as in a planar structure for different interleaving winding arrangements. The analysis is performed in terms of leakage inductance, winding capacitance and winding loss. Efficiency measurements are performed to verify the effect on the converter performance.**

Keywords*— High step-up, stand-alone, LED lighting, tapped-inductor, leakage inductance, stray capacitance.

I. INTRODUCTION

Modern switched-mode power supplies (SMPS) nowadays, are dominated by a trend to achieve both high efficiency and high power density. In order to increase the converters power density, the energy storage requirement plays an important role. One option to reduce the size of the energy storage elements is to increase the converter switching frequency using soft-switching techniques [1], however in hard switched PWM converters the increment in the switching frequency is penalized in the form of increased converter switching losses. This work focusses on evaluating different magnetic structures for a LED lightning application in order to maximize the converter efficiency.

On the one hand, planar magnetics components provide lower profile than conventional wire-wound structures. Moreover, planar magnetic technology provides good thermal characteristics since they present higher surface area, which make them more efficient to conduct heat. Furthermore, lower leakage inductance than conventional structures can be achieved because of improved magnetic coupling and extensive interleaving [2], [3]. All these characteristics make planar magnetics a good candidate for effectively increasing the system power density and efficiency. Moreover, printed circuit boards (PCB) windings offer easier manufacturability and better repeatability than conventional wire-wound magnetic components. On the other hand, planar magnetics present the disadvantage of increased inter-layer capacitance and limited number of turns by the manufacturing process.

The stored energy in the leakage inductance of the magnetic component causes undesirable overvoltage spikes on the drain of the main switch at turn off, which leads to increased switching losses. On the other hand, applications with high voltage stress will suffer from large stray capacitances in the magnetic structure, which can lead to undesirable resonating current spikes and consequently large capacitive switching losses. In this work an analysis and comparison of magnetics structures in a tapped boost converter for LED applications is performed. The aim is to compare different winding arrangements in a conventional wire-wound structure in terms of leakage inductance, winding capacitance and winding loss. The results are compared to the possible advantages attained by using planar magnetics instead of conventional wire-wound structures. The magnetic component is a coupled inductor, which is analyzed in a conventional wire-wound core ETD for full interleaving, partial interleaving and no interleaving and compared to a planar structure ELP with full interleaving winding arrangement.

II. SYSTEM ANALYSIS AND SPECIFICATIONS

The application under analysis is a stand-alone photovoltaic LED lamp system with a lithium battery for energy storage. The photovoltaic panel is formed by two parallel-connected monocrystalline panels. The integrated battery is a LiFePO4 (lithium iron phosphate) battery from GWL Power with a nominal voltage of 3.2 V and a capacity of 15 Ah. The LED lamp is composed of eight series-connected Cree XLamp XP-E. Fig. 1 shows the LED lamp I-V curve extracted from the component datasheet and Table I presents the specifications of the PV-LED system.

Three port converter topologies (TPC) for renewable energy systems [3] have been recently introduced. These topologies claim to provide higher efficiency and power density than conventional cascaded structures [4] due to reduced conversion stages. However, it is required to add extra switches to provide controllability and/or diodes to configure the power flow path. Therefore, TPC topologies need a high number of semiconductors, which directly influences the system efficiency and power density. Figure 2 shows the block diagram of the TPC structure and the conventional cascade converters in a light to light (LtL) system. In this work the conventional cascaded structure is preferred since it features lower number of components and easier implementation of the control scheme of the maximum power point tracking (MPPT) and battery management system (BMS) than TPC topologies.

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TABLE I
PV-LED SYSTEM SPECIFICATIONS

P_{PV_mp}	$10.92\ W$
V_{mp}	$6.50\ V$
I_{mp}	$1.68\ A$
V_{oc}	$8.10\ V$
I_{sc}	$1.86\ A$
$V_{bat-nom}$	$3.2\ V$
R_{bat}	$\leq 9\ m\Omega$
LED	$8\ x\ [2.6-3.3]\ V_{fw}$

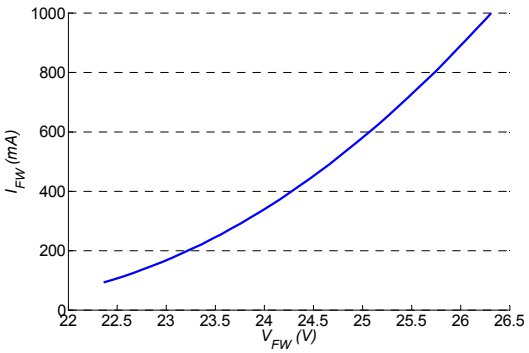

Fig. 1 LED lamp $I-V$ curve (8 series-connected LED Cree XLamp XP-E)

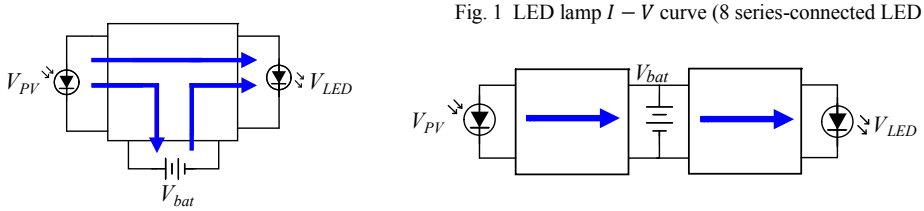

Fig. 2 Light to Light (LtL) three port converter TPC (left) and cascaded solution (right)

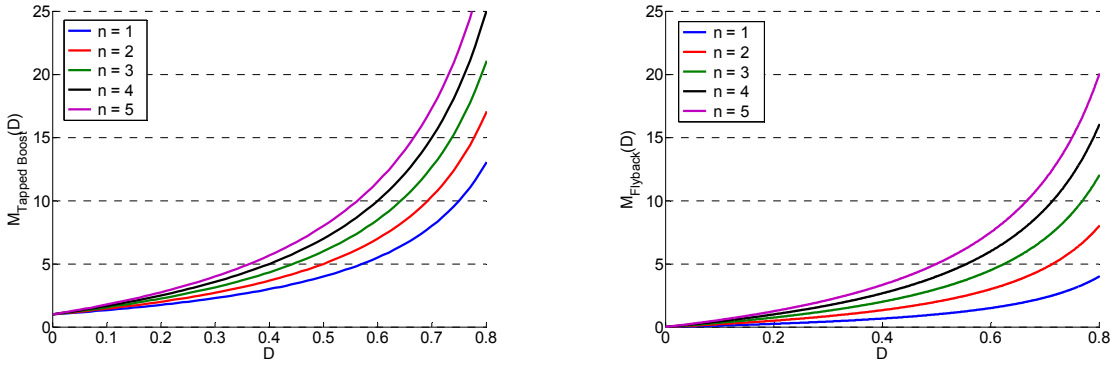

Fig. 3 Tapped boost topology (left) and flyback converter (right) input to output voltage gain

The topology selected for the LtL system is a buck converter from the photovoltaic panel to the battery and a tapped boost converter from the battery to the LED port connected in series. In order to drive the LED light from the battery port, a high voltage conversion ratio is needed. The use of tapped inductors provides high step-up ratio, which makes it possible to avoid extreme duty cycles and high current stress in the components reducing switching and conduction losses [5], [7]. The tapped boost converter achieves high transformation ratio with low amount of components and present higher voltage gain than the flyback topology as shown in Fig. 3. Fig. 4 (a) shows the buck and tapped boost converters series-connected and (b) shows the operating waveforms of the tapped boost converter. During the first subinterval switch M_2 is active and inductor L_2 is charging with a rate determined by the battery voltage and the inductor value. When switch M_2 is turned off, the synchronous rectifier SR_2 turns on and the energy is transferred to the load through the series combination of the inductors L_2 and L_3. The dc voltage transfer function of the tapped boost is obtained from the inductor volt-second balance as shown in (1) and (2).

$$V_{bat} \cdot D_2 T + \left(\frac{V_{bat} - V_{LED}}{n+1}\right) \cdot (1 - D_2)T = 0 \qquad (1)$$

$$V_{LED} = V_{bat}\left(\frac{1 + nD_2}{1 - D_2}\right) \qquad (2)$$

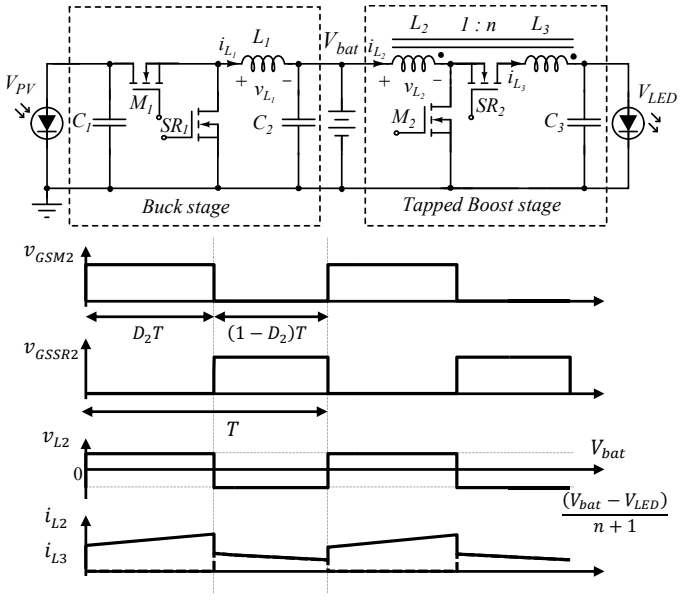

Fig. 4 a) LtL Buck and tapped boost converters series-connected. b) Tapped boost converter operating waveforms: gate to source voltage of switches M_2 and SR_2, inductor L_2 voltage and inductor L_2 and L_3 current, continuous and dotted line.

III. Leakage Inductance, AC Resistance and Stray Capacitance

The different magnetic structures are evaluated taking into account the leakage inductance between the coupled inductors, the parasitic capacitance and the ac resistance. All these components will have a negative effect on the converter efficiency and need to be carefully evaluated.

The leakage inductance is produced by the fact that the flux linkage between two windings is never complete. According to [8] the leakage inductance can be calculated from the energy stored in the magnetic field of the leakage flux. The stored energy in each layer can be found integrating across the cross sectional area of the layer as given by (3). By using (4) the energy stored in the magnetic field can be calculated as in (5).

$$E = \frac{1}{2} \cdot \int B \cdot H \cdot dV = \frac{1}{2} \cdot L_{lk} \cdot {I_p}^2 \tag{3}$$

$$B = \mu_0 \cdot H \tag{4}$$

$$E = \frac{\mu_0}{2} \cdot \int_0^h H^2 \cdot l_w \cdot b_w \cdot dx \tag{5}$$

Where μ_0 is the vacuum permeability, B is the magnetic flux density, H is the magnetic field strength, I_p is the peak current in the winding, l_w is the mean length turn, b_w is the width of the layer and h is the thickness of the layer. The magnetic field strength is equal to the total current passing through the interior of the total flux path as given by (6).

$$H = \frac{I}{l_m} \tag{6}$$

Where l_m is the magnetic path length. If interleaving is used in the structure, the effective magnetic field strength in each of the layer can be considerably reduced. Planar magnetics can help to reduce the component leakage inductance because they make possible to apply extensive interleaving.

On the other hand, the conduction losses due to the winding resistance dramatically increases with frequency due to eddy currents losses (skin and proximity effect). The dc resistance can be calculated according to (7).

$$R_{dc} = \rho \cdot \frac{N \cdot l_w}{b_w \cdot h} \tag{7}$$

Where N is the number of turns and ρ the resistivity of copper at room temperature. The value of ac resistance can be obtained by using Dowell's equation [9] as shown in (8). Dowell curves give the relation between ac and dc resistance for different layers as shown Fig. 5. The value of ac resistance will depend on the m value for each layer, where m can be calculated as the ratio of magneto motive forces (MMFs) to ampere-turns of the actual layer as shown in (9).

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2}\left[\frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi}\right] \tag{8}$$

$$m = \frac{F(h)}{F(h) - F(0)} \tag{9}$$

Where $\xi = h / \delta$ is the ratio between the copper thickness and the skin depth given by $\delta = \sqrt{\rho / \pi \mu_0 f}$.

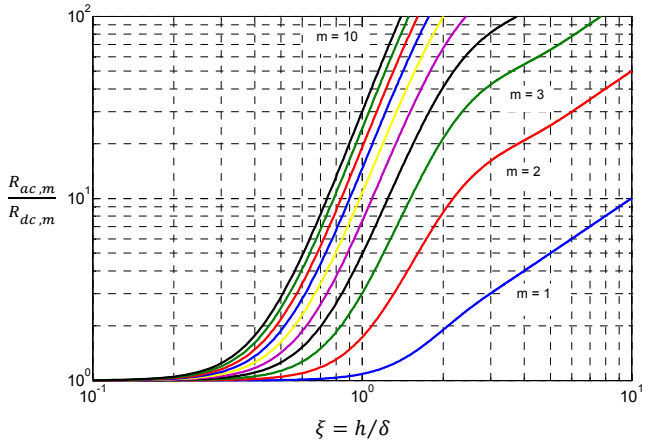

Fig. 5 Dowell's curves. Ratio of ac to dc winding resistance as a function of the conductor thickness and skin depth and number of layers

The value of the inter-winding and intra-winding capacitances can be calculated according to [10] as shown in (10). The electro static energy stored in the capacitance is given by (11).

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d} \tag{10}$$

$$E = \frac{1}{2} \cdot C \cdot V^2 \tag{11}$$

Where ε_0 is the vacuum permittivity, ε_r is the relative permittivity of the dielectric material, A and d are the capacitor plates area and distance respectively and V is the total voltage across the winding.

To perform a fair comparison structures with similar core volume are selected. The wire-wound structure core is an ETD29/16/10 with an effective volume of $V_e = 5350\ mm^3$ and the planar structure is an ELP32/6/20 with an effective volume of $V_e = 5390\ mm^3$ both in material N87 from EPCOS. The inductance value and number of turns in each magnetic structure are selected to produce approximately the same core losses. The core losses are calculated using Modified Steinmetz Equation (MSE) according to [11] as shown in (12), (13) and (14). The calculated core losses are 5.6 mW for the ELP and 4.5 mW for the ETD structure, with 4 and 7 turns respectively and a transformation ratio 1:5.

$$P_{MSE} = K \cdot {f_{eq}}^{\alpha - 1} \cdot \left(B_{pk}\right)^{\beta} \cdot f \quad (mW/cm^3) \tag{12}$$

$$f_{eq} = \frac{2}{\Delta B^2 \cdot \pi^2} \cdot \int_0^T \left(\frac{dB}{dt}\right)^2 dt \tag{13}$$

$$\Delta B = \frac{V_{bat}}{N \cdot A_e} D_2\, T \tag{14}$$

Where K, α and β are the Steinmetz coefficients, f is the frequency, B_{pk} is the peak ac flux density, ΔB is the peak to peak ac flux density and A_e is the effective area of the core.

The PCB windings are implemented using 270 μm copper thickness in 8 layers using full interleaving technique (PSPSPSPS). Two PCB stacks are connected in parallel which helps to reduce the dc resistance. The copper thickness of the wire-wound structures ($d = 0.70\ mm$) is selected to have approximately the same copper volume than the planar magnetics PCB windings.

Fig. 6 Coupled inductors in planar magnetics ELP32/6/20 (left) and wire-wound structure ETD29/16/10 core (right) for different winding arrangements

TABLE II
COUPLED INDUCTORS MEASURED PARAMETERS @ 20 KHZ

$Core\ Type - n_{pri}/n_{sec}\ (Winding\ arrangement)$	$L_2\ (\mu H)$	$L_{lk}\ (nH)$	$C_p\ (nF)$	$C_{pri-sec}\ (nF)$
$ETD29 - 7/35\ (PSPS)$	18.64	87.20	0.50	0.19
$ETD29 - 7/35\ (PSSP)$	19.48	97.44	1.04	0.15
$ETD29 - 7/35\ (PPSS)$	18.7	199.20	0.73	0.07
$ELP\ 32 - 4/20 - 2\ PCB\ parallel\ (PSPSPSPS)$	18.56	18.40	4.95	2.78

In order to use the full window width of the ETD structure each of the primary layers is formed by 3 windings in parallel. The copper volume is calculated as $V_{cu} = 1523\ mm^3$ for the ELP structure and $V_{cu} = 1551\ mm^3$ for the ETD core. The implemented winding scheme is U-type, which helps to decrease the distance between windings in order to reduce the structure leakage inductance. However, this arrangement will produce higher capacitive loss than the Z-type winding [12].

Fig. 6 shows the implemented coupled inductors in planar magnetics ELP and conventional ETD wire-wound for different winding configurations. Full interleaving (PSPS), partial interleaving (PSSP), and no interleaving (PPSS) winding arrangements are implemented to compare the effects of the leakage inductance, winding capacitance and winding loss. Table II shows the measured coupled inductor parameters using an Agilent 4294A impedance analyzer. The values are referred to the primary side. The leakage inductance is measured at the secondary side to minimize the error in the measurement. Fig. 7 shows the parasitic capacitances of the tapped-inductor structure. Full interleaving techniques helps reducing the leakage inductance. By interleaving primary and secondary layers the MMF is reduced since each layer effectively operates with $m = 1$. The lowest leakage inductance is achieved with the ELP full interleaving structure. The highest value is given by the ETD core with no interleaving arrangement. On the other hand, the planar magnetics present the highest primary and primary to secondary capacitances, C_p and $C_{pri-sec}$.

Fig. 8 and Fig. 9 show the measured value of the winding resistance as a function of the frequency for the charge and discharge intervals. The measurements are performed with core, therefore they include core and fringing flux loss. The ac resistance cannot be directly extracted from this measurement, however since the couple inductors have been designed to have approximately the same core loss, the measurement allows for a direct comparison of the resistance value of the different structures. The planar structure shows very low dc resistance in both charge and discharge intervals.

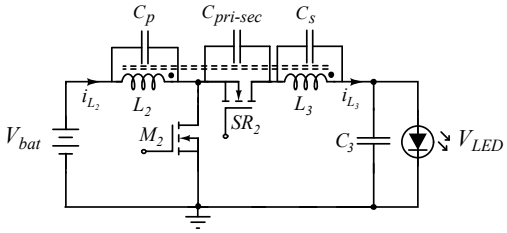

Fig. 7 Tapped-inductor structure stray capacitances

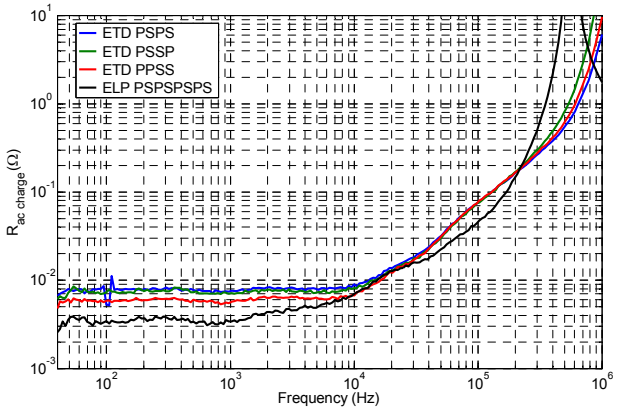

Fig. 8 Coupled inductors measured resistance during the charge interval

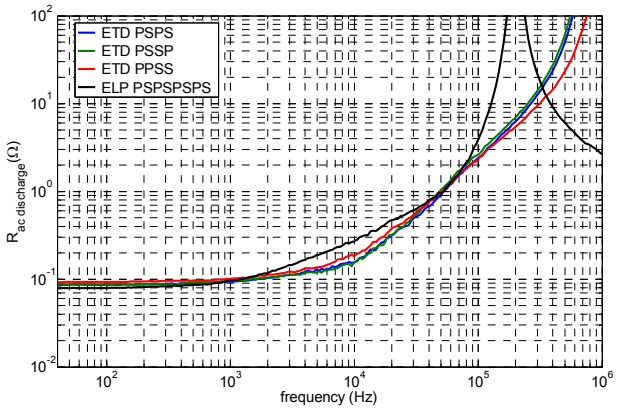

Fig. 9 Coupled inductors measured resistance during the discharge interval

The ELP structure resonance frequency is placed at 500 and 200 kHz for the charge and discharge subintervals respectively. This makes it difficult to compare their ac resistance. However, it is possible to observe that the planar structure at 100 kHz presents the lower charge resistance. On the other hand, the discharge resistance is similar in all the implemented structures.

IV. Experimental Results

Fig. 10 shows the implemented prototype, where the magnetic components are placed at the bottom side of the board. The converter operating frequency is 100 kHz. The power stage is controlled by a 16 bit low power consumption microcontroller from Texas Instruments MSP430F5172. Fig 11 shows the converter operating waveforms with the wire-wound coupled inductors and no interleaving winding arrangement (PPSS). Fig. 12 shows the converter operating waveforms with the planar magnetics structure and full interleaving winding arrangement (PSPSPSPS). The effect of the leakage inductance can be observed in the drain to source voltage of the switch M_2. The energy stored in the leakage inductance resonates with the semiconductor and inductor parasitic capacitances, until it is damped as joule loss in the circuit or until the MOSFET enters into avalanche mode. Moreover, the magnetic component parasitic capacitances can be observed at the switch M_2 turn on event. At this event, a change in the energy stored in the parasitic capacitances will generate the same amount of joule energy loss in the MOSFET channel and circuit parasitic resistances.

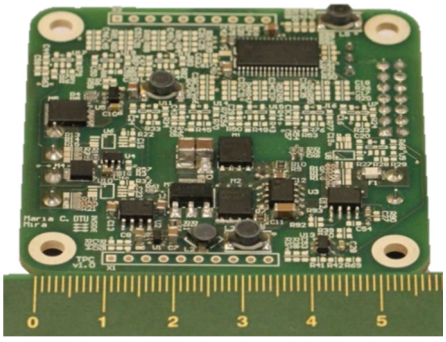

Fig. 10 Tapped boost converter prototype

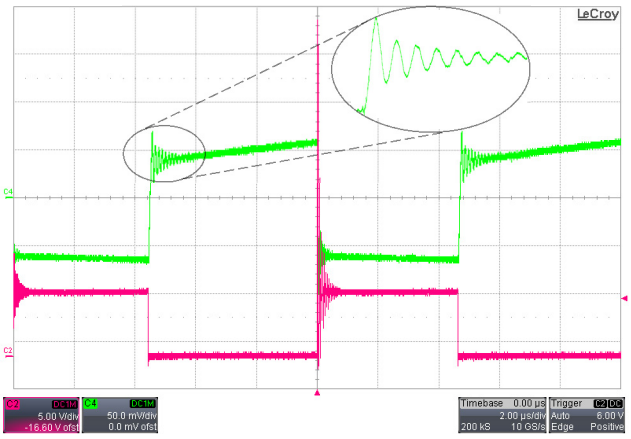

Fig. 11 Tapped boost converter operating waveforms with ETD wire-wound structure and no interleaving winding arrangement (PPSS). Red trace: switch M_2 drain to source voltage (5V/div). Green trace: inductor current (2.5A/div) measured with a Rogowski coil (20mV/A, 125x). Time scale 2µs/div.

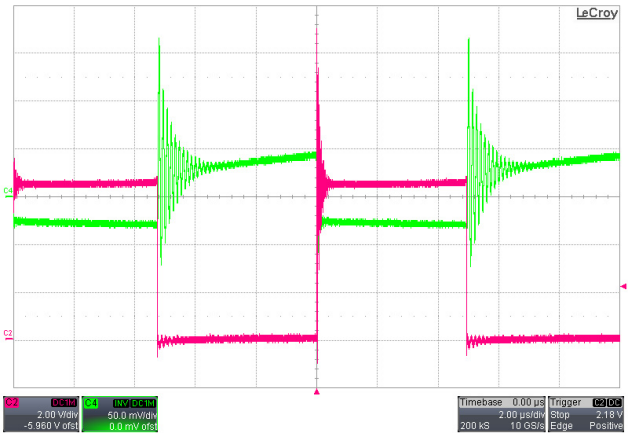

Fig. 12 Tapped boost converter operating waveforms with ELP planar magnetics structure and full interleaving winding arrangement (PSPSPSPS). Red trace: switch M_2 drain to source voltage (2V/div). Green trace: inductor current (2.5A/div) measured with a Rogowski coil (20mV/A, 125x). Time scale 2µs/div.

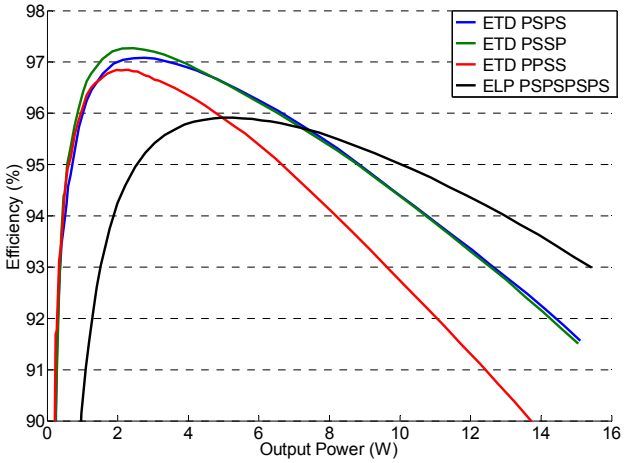

Fig. 13 Tapped boost converter efficiency measurements for different magnetic structures and winding arrangements

Fig. 13 shows the tapped boost converter efficiency measurements for the different structures and winding arrangements. The measurement is performed with 6.5 digit precision multimeters Agilent 34410A and it only includes the power stage losses. From the efficiency measurements the effects of the different parasitics on the converter performance can be observed. The ETD structures with lower stray capacitance than the planar structure present lower capacitive loss. This effect can be observed in the efficiency curves at low power levels where capacitive losses are predominant. After the efficiency peak and as the power level increases the effect of the winding losses and leakage inductance become predominant. The ETD structure with no interleaving presents the lowest efficiency at high power levels since it presents the highest leakage inductance. The ETD structures with full and partial interleaving present similar parasitics values and efficiency curves. The highest efficiency is achieved with the ETD structure with partial interleaving technique (PSSP). Is only at high power levels where the lower ELP leakage inductance gives an efficiency improvement. Due to the high step-up voltage in this application, the inter-winding capacitance $C_{pri-sec}$ is subjected to high voltage stress. The large inter-winding capacitance in the ELP structure causes a large efficiency degradation at low power levels compared to the ETD structures.

In order to evaluate how the capacitive loss affect the total efficiency, the energy loss can be calculated applying (11) and using the stray capacitance measurements from Table II as shown in (15) and (16).

$$E_{C_{pri}} = \frac{1}{2} \cdot C_{pri} \cdot \left({V_{bat}}^2 + \left(\frac{V_{LED} - nV_{bat}}{n+1} \right)^2 \right) \quad (15)$$

$$E_{C_{pri-sec}} = \frac{1}{2} \cdot C_{pri-sec} \cdot (V_{LED} + nV_{bat})^2 \quad (16)$$

However, the measured primary to secondary capacitance $C_{pri-sec}$ corresponds to the capacitance between windings with both of the windings shorted. In the real circuit only the capacitance between the winding turns placed closer to the MOSFET and the synchronous rectifier switching nodes will store most of the inter-winding parasitic capacitance energy. In order to take this into account, the value of this parasitic component is calculated from the self-resonance frequency of the inductor current at the MOSFET turn on event. The calculated inter-winding capacitance values are $520.09\ pF$ and $65.97\ pF$ for the ELP and ETD structures, respectively.

Fig. 14 shows the calculated capacitive power loss of the tapped boost converter working with the planar ELP structure (full interleaving) and with the wire-wound ETD structure (no interleaving). The capacitive loss due to the primary capacitance (C_{pri}) is plotted in blue and black lines for the ELP and ETD structures, respectively. The primary to secondary capacitive loss ($C_{pri-sec}$) is shown in green and red lines for the planar and the wire-wound structures, respectively. It can be observed that the losses due to the primary stray capacitance are very small compared to the loss due to the inter-winding capacitance. This is due to the high voltage stress in this parasitic component. The planar magnetics present high stray capacitance losses, which deteriorate the converter performance at low power levels. At $2\ W$ output power, the inter-winding capacitive loss of the ELP structure corresponds to 30 % of the total converter loss. The wire-wound ETD structure at $2\ W$ output power represents 7 % of the total power loss. As the power level increases, the contribution of the capacitive loss decreases and the major source of loss comes from the ac resistance and the leakage inductance.

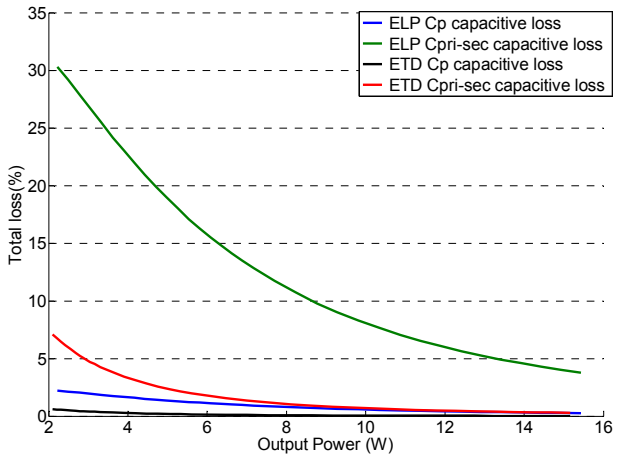

Fig. 14 Calculated capacitive loss of the tapped boost converter with the ELP structure (full interleaving) and with the wire-wound ETD structure (no interleaving)

V. Conclusions

This work presents an experimental evaluation and comparison of conventional wire-wound structures and planar magnetics with PCB windings for a high step-up ratio tapped boost converter. The converter application is a stand-alone LED lighting and the magnetic structure evaluation is performed with the aim of maximizing the converter efficiency. Different winding arrangements are evaluated in terms of leakage inductance, winding resistance and stray capacitances. Efficiency measurements show the influence of the different parasitics on the converter performance. The experimental results shows that the planar structure is only a valid candidate for optimizing the converter at high output power levels where leakage inductance is the predominant cause of loss. However, at low power levels the conventional ETD wire-wound structures are preferred compared to the planar solution due to the smaller parasitic capacitances. Moreover, conventional wire-wound structures make it possible to apply Z-type winding technique to further reduce stray capacitances.

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